

Application/Control Number: 10/748,273

Page 2

Art Unit: ***

PTOCLM

12/31/03

AS

CLAIMS 1-11 (CANCELLED)

Art Unit: ***

BEST AVAILABLE COPY

12. A method of manufacturing a semiconductor device comprising steps of:

(a) preparing an SOI substrate formed by a semiconductor substrate <1>, an embedded insulating layer <2> and an SOI layer <3>;

(b) selectively forming an isolation film <31> in an upper layer part of said SOI layer while forming a first conductivity type semiconductor region <11, 12> in a lower layer part of said isolation film so that said isolation film separates said SOI layer into a plurality of element forming regions and at least one said element forming region has a first conductivity type and is formed in contact with said semiconductor region among said plurality of element forming regions;

(c) selectively forming a second conductivity type active region <5, 6> on the surface of said at least one element forming region; and

(d) forming a first conductivity type body region <10> capable of being externally fixed in electric potential in said SOI layer to be in contact with said semiconductor region, wherein

said step (c) is carried out for forming said active region by setting a block region <41 to 45> including said body region and a partial region of said isolation film to a region inhibiting introduction of an impurity of said second conductivity type and introducing said impurity of said second conductivity type into said SOI layer.

13. The method of manufacturing a semiconductor device according to claim 12, wherein

said step (c) includes a step of introducing an impurity of said second conductivity type into said SOI layer through a mask of a first resist film <51, 52> formed on said block region.

Art Unit: ***

BEST AVAILABLE COPY

14. The method of manufacturing a semiconductor device according to claim 13, wherein

said at least one element forming region includes a region for forming a transistor,

said method further comprising:

(e) a step executed in advance of said step (c) for forming a gate electrode <9> of said transistor on said at least one element forming region, said gate electrode being formed to extend on said isolation film,

said step (c) including a step of introducing an impurity of said second conductivity type into said SOI layer through masks of said first resist film and said gate electrode.

15. The method of manufacturing a semiconductor device according to claim 14, wherein

said first resist film and said gate electrode are continuously formed on a region reaching said at least one element forming region from said body region.

16. The method of manufacturing a semiconductor device according to claim 12, wherein

said at least one element forming region includes a region for forming a transistor,

said method further comprising:

(e) a step executed in advance of said step (c) for forming a gate electrode <9> of said transistor on said at least one element forming region, said gate electrode being

Art Unit: ***

formed to extend on part of said isolation film,

said step (c) including a step of introducing an impurity of said second conductivity type into said SOI layer through masks of a first resist film formed on said body region and said gate electrode.

17. The method of manufacturing a semiconductor device according to claim 16, wherein

said gate electrode is formed on a region reaching said at least one element forming region from said body region.

18. The method of manufacturing a semiconductor device according to claim 12, wherein

said step (c) includes a step of introducing an impurity of said second conductivity type into said SOI layer through a mask of a first resist film <62> having a first opening on said active region, and

said step (d) includes a step of introducing an impurity of said first conductivity type into said SOI layer through a mask of a second resist film <61, 63> having a second opening on said body region.

19. The method of manufacturing a semiconductor device according to claim 18, wherein

said second opening includes an opening provided substantially only on said body region.

20. The method of manufacturing a semiconductor device according to claim

BEST AVAILABLE COPY

Art Unit: ***

BEST AVAILABLE COPY

18, wherein

said second opening includes an opening provided on said body region and part of said isolation film.

21. The method of manufacturing a semiconductor device according to claim 20, wherein

said second opening includes an opening provided on a region reaching said at least one element forming region from said body region.

22. The method of manufacturing a semiconductor device according to claim 18, wherein

said first resist film further has a first dummy opening <71> on a region other than said body region, said semiconductor region and said at least one element forming region, and

said second resist film further has a second dummy opening <72> on a region other than said body region, said semiconductor region and said at least one element forming region.

23. The method of manufacturing a semiconductor device according to claim 22, wherein

said first and second dummy openings are formed on the same position in the same shape.

24. The method of manufacturing a semiconductor device according to claim 22, wherein

Art Unit: ***

said first and second dummy openings are formed without overlapping with each other.

BEST AVAILABLE COPY